

Curriculum vitae: SIVA SATYENDRA SAHOO

PERSONAL DETAILS

NAME:	Siva Satyendra Sahoo
GENDER:	Male
PLACE AND DATE OF BIRTH:	Dhuturdah SHC, India 15 November 1985
ADDRESS:	0202, Erasme Ruelensvest 37, Heverlee-3001, Belgium
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FAMILY STATUS:	Married
DATE OF CV:	July 18, 2026

DEGREES

06/2019	DOCTORATE DEGREE, Doctor of Philosophy (Ph.D.) 4 Engineering Drive 3, National University of Singapore, Singapore 117583 Grade: 4.0/5.0
01/2015–02/2019	PhD Scholar at Department of Electrical and Computer Engineering Thesis: <i>A Cross-layer Reliability-integrated System-level Design Methodology for Heterogeneous Multiprocessor SoC-based Embedded Systems</i> . The thesis involved research into optimizing the distribution of reliability methods across multiple layers of the system stack during both design-time and run-time.
09/2012	MASTER'S DEGREE, Master of Technology (M.Tech) Indian Institute of Science, Bangalore, India Grade: First Class (6.6/8.0)
07/2010–06/2012	Electronics Design and Technology Project: <i>Hardware Accelerator for Support Vector Machines</i> . The project aimed at accelerating the training phase of Support Vector Machine using FPGAs for hardware/software co-design.
12/2008	BACHELOR'S DEGREE, Bachelor of Technology (B.Tech) Biju Patnaik University of Technology, Rourkela, India (College of Engineering and Technology, Bhubaneswar, India) Grade: 8.65/10.0
07/2004–06/2008	Instrumentation and Electronics Engineering Project: <i>Short Message Service (SMS)-based Home Automation</i> . The project work involved the implementation of a wireless embedded system, using a mobile phone or a GSM modem, for the purpose of automation and control.

CERTIFICATIONS

• Neural Networks and Deep Learning, DeepLearning.AI (Coursera) 2017
• Mathematics for Machine Learning, Imperial College London (Coursera) 2018
• R Programming, Johns Hopkins University (Coursera) 2017

LANGUAGE SKILLS

ENGLISH	Full professional proficiency
ODIA	Native proficiency
HINDI	Limited working proficiency

CURRENT EMPLOYMENT

since 01/2023	Senior Researcher, Pathfinding Semiconductor Technologies (PSTe), Interuniversity Microelectronics Centre (IMEC), Leuven, Belgium Individual contributor to the exploration of technology-aware architecture design for executing workloads at varying scales of computation. The project explores the impact of semiconductor technology innovations on system-level design and provides feasible directions for future technological innovations. One of the aspects being explored actively pertains to the investigation into the impact of provisioning <i>high-capacity on-chip memory</i>, using <i>novel devices/3D integration/heterogeneous integration</i>, for a variety of emerging workload scenarios. Further, one of the research projects involves investigating the design and implementation of the next generation of reconfigurable systems, leveraging novel device and integration technologies. It presents a complex research problem that spans semiconductor technology, computer architecture, and emerging workloads.
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PREVIOUS WORK EXPERIENCE

08/2021–12/2022	Senior Staff Engineer, AI Computing, SAIT, Samsung Semiconductor India Research, Bangalore, India Individual contributor for modeling and DSE of AI computing architectures. Collaborator in the analysis and optimization of mapping AI workloads on modern inference engines.
02/2019–07/2021	Post-doctoral Researcher, Chair for Processor Design, Computer Science Department, Technische Universität Dresden, Germany. Subject matter expert and collaborator for various research projects involving Electronic System-level (ESL) design, AI/ML for Electronic Design Automation (EDA), and embedded machine learning design. Co-instructor for Embedded Hardware System Design course. Supervisor (and co-supervisor) for research interns
08/2012–12/2014	Digital Design Engineer, Intel India, Bangalore, India Worked in the domain of <i>Physical Design</i> of dense VLSI System-on-chip. Was primarily responsible for design quality assessment of full-chip as well as design blocks.
07/2008–03/2010	Assistant Systems Engineer, Tata Consultancy Services, India. Worked in the domain of <i>Business Intelligence and Performance Management</i>. Primarily involved in using state-of-the-art tools for integrating data from heterogeneous sources for data analysis.

RESEARCH FUNDING AND GRANTS

JAN. 2017	HiPEAC Collaboration Grants , HiPEAC4 Network of Excellence
2015 – 2018	NUS Graduate Scholarship , National University of Singapore, Singapore.

RESEARCH OUTPUT

Peer-reviewed Journals	Number of publications: 15 Authored articles for top journal publications including IEEE Transactions on Computers, IEEE Access, and ACM Transactions on Embedded Computing Systems
Peer-reviewed Proceedings	Number of publications: 28 Have been regularly presenting research results at top conferences in the field of electronic system design, including ICCAD, DAC, DATE, and ASP-DAC.
Book Chapters	Number of publications: 4 Have authored/co-authored two chapters for the Springer Handbook on Computer Architecture.

Open-source Contributions	AxOSyn – Approximate Operator & DSE Toolkit A Python toolkit for modeling, characterizing, and exploring approximate arithmetic operators and their impact on PPA (performance/latency, energy/power, area/LUTs) and behavioral accuracy.
	Approximate Operator Designs The results of the research on approximate computing led to providing a library of approximate operator designs for FPGA-based systems.
Research Tutorial	Co-presenter, Design, Model & Explore Approximate Arithmetic Circuits: A Tutorial, ESWEEK 2025 Contributed to a tutorial on the design, modeling, and exploration of approximate arithmetic circuits.
	Co-developer, Tutorial on Enabling Design Automation in Xilinx Partial Reconfiguration Design Flow, FPL 2018 Contributed to a tutorial on HW/HW partitioning for partially reconfigurable systems in FPGAs-based HMPSoCs.

RESEARCH SUPERVISION

Navya Agarwal	Masters Thesis, <i>Circuits for Novel Reconfigurable Systems</i> TU Delft. Research Intern at IMEC, Leuven. 2025-26
Joswin Dsouza	Masters Thesis, <i>FPGA Architecture Exploration</i> Université de Montpellier. Research Intern at IMEC, Leuven. 2025
Xunqin Lai	Masters Thesis, <i>FPGA Architecture Exploration for SNN Workloads</i> TU, Eindhoven. Research Intern at IMEC, Leuven. 2023-24
Nemath Ahmed	Bachelors Thesis in <i>Reinforcement Learning for Cyberphysical Systems</i> IIT, Indore. Guest Researcher at TU, Dresden, Germany. 2021
Divyansh Choudhary	Bachelors Thesis in <i>Modeling Deep RL Accelerators</i> , IIT, Indore. Guest Researcher at TU, Dresden, Germany. 2021
Amritha Immaneni	Bachelors Thesis in <i>Posit-based Approximate Arithmetic Hardware</i> , BITS Pilani, Hyderabad. Guest Researcher at TU, Dresden, Germany. 2021
Debabrata Chaudhury	Bachelors Thesis in <i>Bio-medical Signal processing for Edge Systems</i> , BITS Pilani, Pilani. Guest Researcher at TU, Dresden, Germany. 2021
Akhil Raj Baranwal	Bachelors Thesis in <i>Accelerator Design for Q-Learning</i> , BITS Pilani, Hyderabad. Guest Researcher at TU, Dresden, Germany. 2020
Suresh Nambi	Bachelors Thesis in <i>Hybrid Arithmetic for ANNs</i> , BITS Pilani, Pilani. Guest Researcher at TU, Dresden, Germany. 2020
Nisarg Sheth	Bachelors Thesis in <i>Cross-layer Energy Optimization</i> , BITS Pilani, Goa. Guest Researcher at TU, Dresden, Germany. 2020
Kshitij Shrivastava	Bachelors Thesis in <i>BIST insertion for Reliable FPGA-based Systems</i> , BITS Pilani, Hyderabad. Guest Researcher at TU, Dresden, Germany. 2018

TEACHING MERITS

Co-instructor	Computer Science Department, TU Dresden, Germany EHSD - Embedded Hardware System Design
Instructor	Computer Science Department, TU Dresden, Germany (Forschung)Praktikum EHSD - (Research)Practical EHSD
Graduate Assistant	Department of Electrical and Computer Engineering, NUS, Singapore EE 4218 - Embedded Hardware Systems Design EE 4214 - Real-time Embedded Systems EE 5903 - Real-time Systems EE 2020 - Digital Fundamentals
Teaching Assistant	School of Continuing and Lifelong Education, NUS, Singapore TE 3801 - Robust Design of Electronic Circuits TE 2101 - Programming Methodology

AWARDS & HONOURS

2010 – 2012	MHRD (GATE) Scholarship , Government of India, India
2004 – 2008	CET Merit Scholarship , CET, Bhubaneswar, India.

MISCELLANEOUS ACADEMIC MERITS

ASSOCIATE EDITOR	IEEE Embedded System Letters (ESL), 2024-
MEMBER OF TPC	Design, Automation and Test in Europe Conference (DATE), 2026, 2027 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2025, 2026 ACM/IEEE International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), ESWEEK 2025, 2026 IEEE International Conference on Computer Design (ICCD), 2023
PEER REVIEWER	Regular reviewer of articles for conferences (DATE, DAC, ICCD, ISCAS etc.) and journals (IEEE TETC, IEEE TVLSI, IEEE ESL etc.).

REFERENCES

Akash Kumar	Professor, Embedded Systems, Faculty of Electrical Engineering and Information Technology, Ruhr University Bochum, Germany. Akash.Kumar@rub.de
Salim Ullah	Group Leader, Embedded Systems, Faculty of Electrical Engineering and Information Technology, Ruhr University Bochum, Germany. Salim.Ullah@rub.de
Bharadwaj Veeravalli	Associate Professor, Communication and Networks, Department of Electrical and Computer Engineering, National University of Singapore, Singapore. elebv@nus.edu.sg